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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/090,585	02/28/2002	Peter Breger	1582-US	5017

7590 09/16/2003

Legal Department
Teradyne, Inc.
321 Harrison Avenue
Boston, MA 02118

EXAMINER
WACHSMAN, HAL D

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 09/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/090,585	BREGER ET AL.	
	Examiner	Art Unit	
	Hal D Wachsman	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.

EXAMINER

ART UNIT	PAPER
	3

DATE MAILED:

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Commissioner for Patents

Hal D Wachsman
Primary Examiner
Art Unit: 2857

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the method (see claim 5) of testing a plurality of semiconductor devices (such as in a flow chart for example) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. Page 1, line 25, of the specification with respect to Figure 1, refers to block 14 of this figure as "pattern generation circuitry . However, in Figure 1 block 14 is labeled as "data circuitry". Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1, line 4, cites "a computer workstation" which dangles in the claim because there is no connection between the computer workstation and the other features in claim 1. The last 2 lines of claim 1 cite "...to generate tester waveforms in accordance with the per-pin data" but in accordance in what way ? Claim

5, line 7, cites "applying the test signals..." however the actual antecedent basis is "the unique test data". Claim 5, line 11, cites "certain of the redundant rows and columns" however certain what exactly is being referred to here ? Claim 5, line 5, cites "unique formatting circuitry" however unique in what way ? Claim 5, line 11, cites "the redundant rows and columns" however the actual antecedent basis is "redundant row and column addresses". Claim 5, line 13, cites "the computer workstation" which lacks antecedent basis.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Wada et al. (6,138,257).

As per claim 1, Wada et al. (Abstract, figures 2A, 2B, col. 7 lines 5-9) disclose the computer workstation. Wada et al. (Abstract, col. 5 lines 25, 26, 33, 34, 55-57) disclose "per-pin formatting circuitry having data input circuitry and clock input circuitry". Wada et al. (Abstract, col. 5 lines 20-39, 45-48) disclose "shared timing circuitry coupled to the clock input circuitry....to generate programmed timing signals". Wada et al. (Abstract, col. 6 lines 25-36) disclose "per-pin data circuitry coupled to the

data input circuitry...to generate drive data associated with each individual device pin". Wada et al. (Abstract, col. 5 lines 20-39, 45-48, 55-57, col. 9 lines 44-46, 52-54) disclose "whereby the per-pin formatting circuitry....to generate tester waveforms in accordance with the per-pin data".

As per claim 2, Wada et al. (Abstract, col. 4 line 67, col. 5 lines 24-26, 48-51) disclose the feature of this claim.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada et al. (6,138,257) in view of Aipperspach et al. (6,181,614).

As per claim 3, Wada et al. (Abstract –block 57) disclose the capture memory for storing fail data as described in lines 2-3 of the claim. It appears though that Wada et al. does not clearly disclose the redundancy analyzer circuitry for processing the failure data into a repair solution. However, Aipperspach et al. (see at least abstract) teach this excepted feature. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply the techniques of Aipperspach et al. to the invention of Wada et al. as specified above because as taught by Aipperspach et al. (col. 1 lines 19, 20, 48-52) solid state memory arrays are typically implemented on a semiconductor device and through the use of redundant memory cells, the manufacturing yield of semiconductor devices incorporating memory arrays can be significantly improved, since memory arrays containing relatively minor faults can be repaired, rather than having to be completely scrapped.

As per claim 4, Aipperspach et al. (Abstract, figures 1, 3, 4) teach the feature of this claim. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply the techniques of Aipperspach et al. to the invention of Wada et al. as specified above because as taught by Aipperspach et al. (col. 1 lines 19, 20, 48-52) solid state memory arrays are typically implemented on a semiconductor device and through the use of redundant memory cells, the manufacturing yield of semiconductor devices incorporating memory arrays can be

significantly improved, since memory arrays containing relatively minor faults can be repaired, rather than having to be completely scrapped.

As per claim 5, Wada et al. (Abstract, figure 3, col. 4 lines 66, 67, col. 5 lines 8-12) disclose the generating step. Wada et al. (Abstract, col. 5 lines 20-39, 45-48) disclose the clocking step. Wada et al. (Abstract, figure 3, col. 9 lines 44-46, 52-57, col. 10 lines 1-4, 10-20) disclose the applying step. Wada et al. (Abstract, figure 3) disclose the detecting and storing failure data step. It appears though that Wada et al. does not clearly disclose the remaining features of this claim. However, Aipperspach et al. (Abstract, figures 3, 4, col. 5 lines 1-3, 12-18, 31-43) teach the analyzing step. Aipperspach et al. (Abstract, figure 1, col. 3 lines 20-40) teach the routing step. Aipperspach et al. (Abstract, figures 3, 4, col. 5 lines 1-3, 12-25, 31-43) teach the programming step. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply the techniques of Aipperspach et al. to the invention of Wada et al. as specified above because as taught by Aipperspach et al. (col. 1 lines 19, 20, 48-52) solid state memory arrays are typically implemented on a semiconductor device and through the use of redundant memory cells, the manufacturing yield of semiconductor devices incorporating memory arrays can be significantly improved, since memory arrays containing relatively minor faults can be repaired, rather than having to be completely scrapped.

9. The following references are cited as being art of general interest: Park et al. which disclose row and column redundancy components in a built-in self-repair circuit, Ku which discloses the programming of redundant rows and columns, Bhavsar et al.

which disclose an embedded RAM with self-test and self-repair with spare rows and columns, Turnquist which discloses a wave formatter with pattern and timing generators, Sartschev et al. which disclose per-pin architecture and Brown et al. which disclose an ATE timing measurement unit and method.

10. No claims are allowed.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hal D Wachsman whose telephone number is 703-305-9788. The examiner can normally be reached on Monday to Friday 7:00 A.M. to 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc Hoff can be reached on 703-308-1677. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Hal D Wachsman
Primary Examiner
Art Unit 2857

HW
September 6, 2003